Digital Beamforming design in mmW: A 22nm FDSOI transceiver practical case

Jérôme Prouvée
RF Layout Engineer & Project Manager

IP-SoC Conference 23

FD-SOI for mmW front ends

▶ Let's talk about tech

SiGe BiCMOS
- Best Fmax (RF perf)
- Low integration (digital)

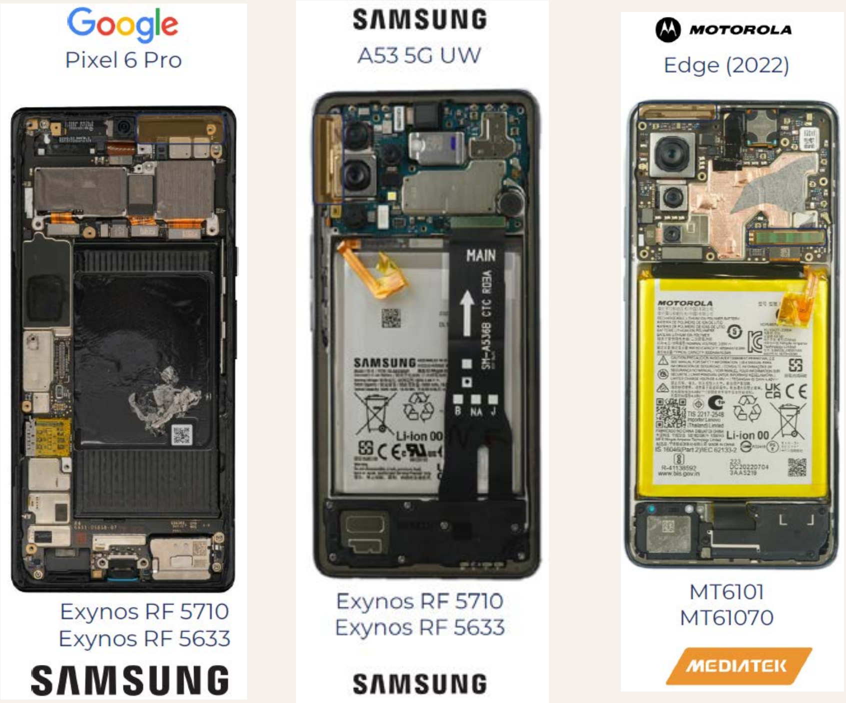
FDSOI CMOS
- Good Fmax
- Good integration (digital)
- Good digital & RF power efficiency

FinFET CMOS
- Low Fmax (RF)
- Best integration (digital)

RF ♥ Digital

FD-SOI

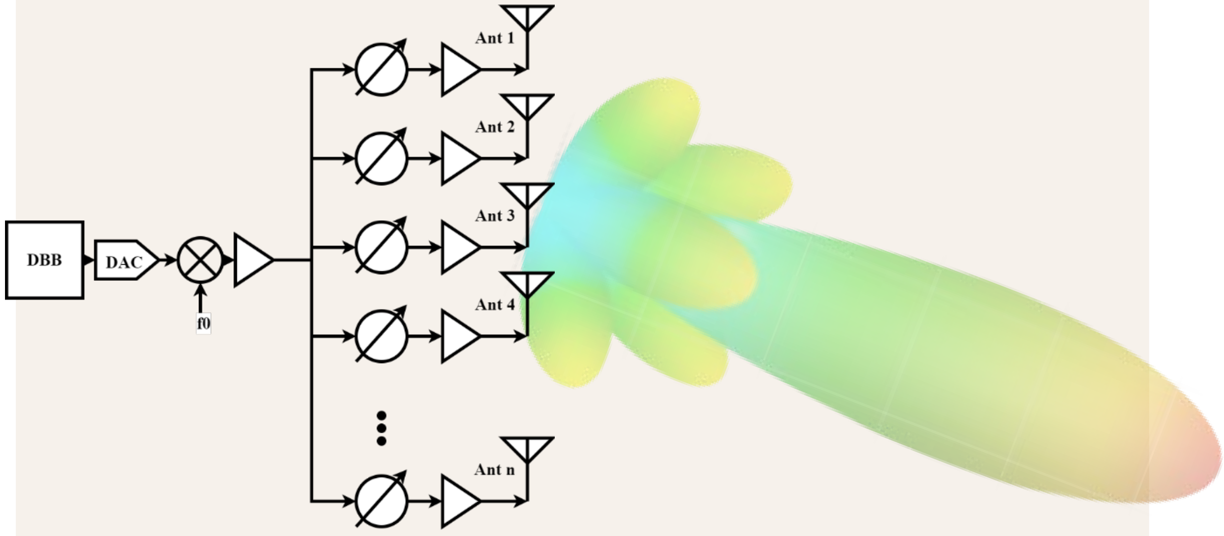
They chose FD-SOI



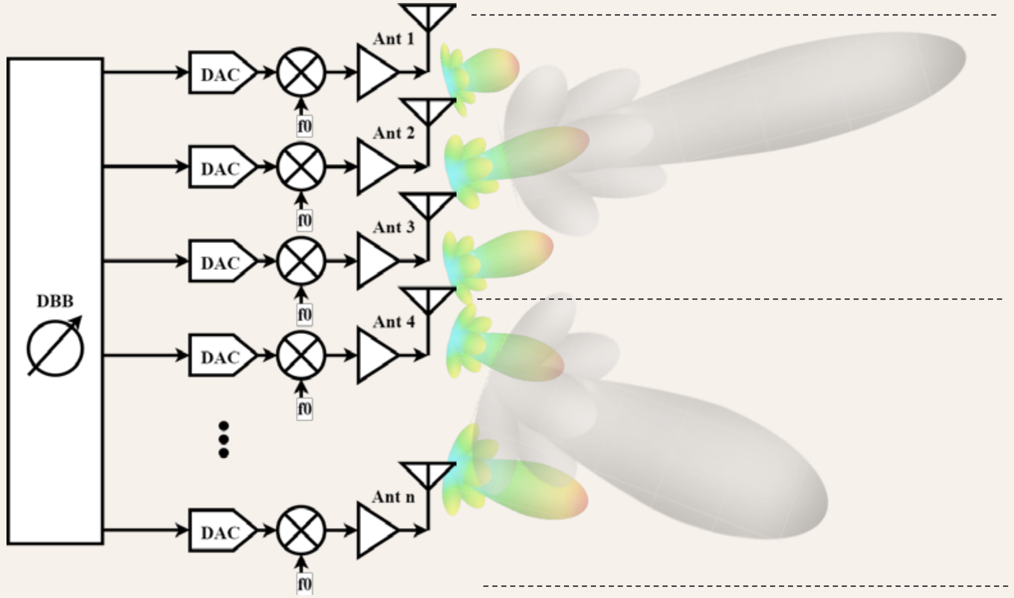
Source: Yole system plus "RF Front-End Module comparison 2023 – 5G mmWave Chipset" Product Brochure

Digital Vs Analog Beamfoming

Analog Beamforming



Digital Beamforming



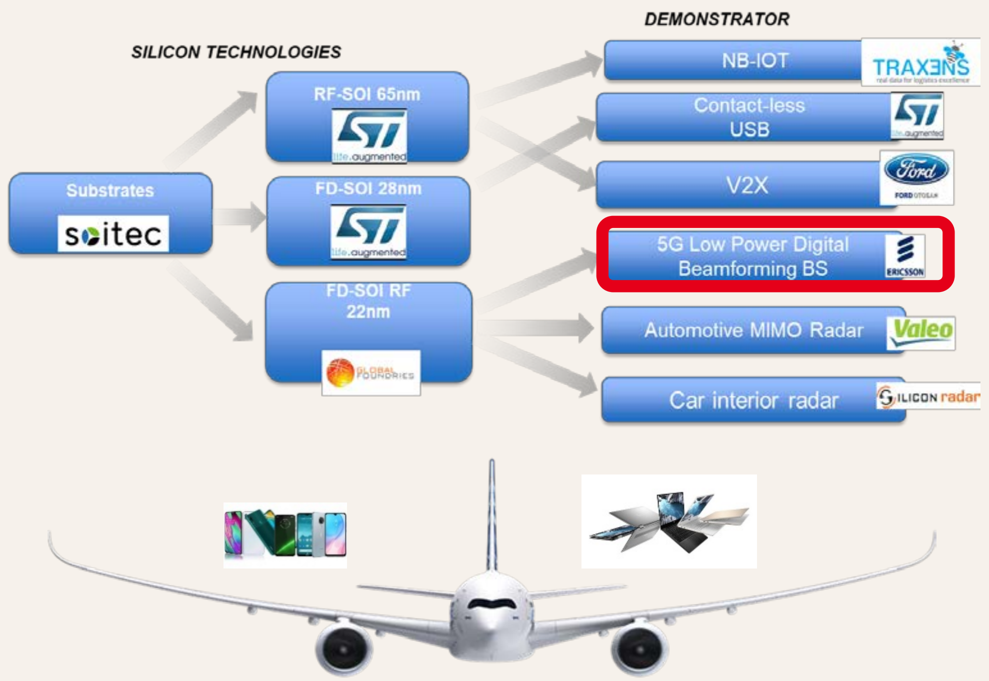
- Simple digital
- Power consumption

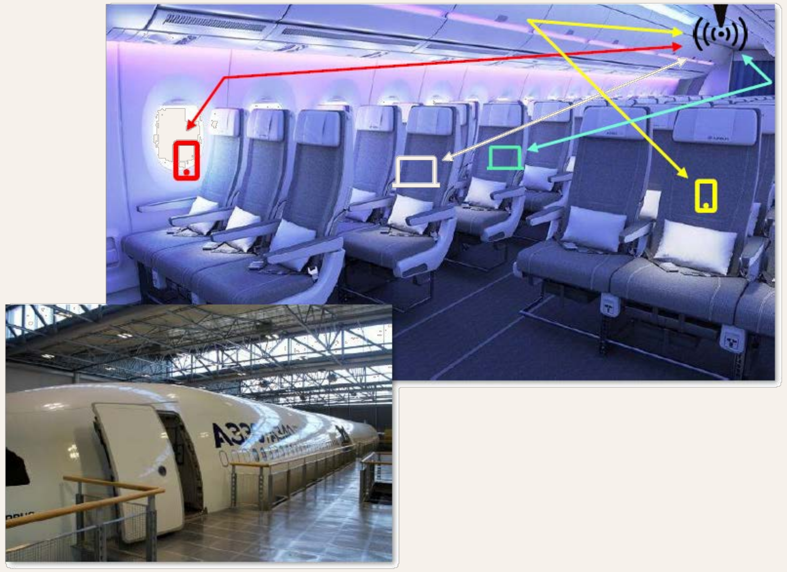
- Single user
- Lossy
- Not flexible

- Multi user & Versatile
- Relax Analog
- Amplitude weighting (selectivity + predist.)

- Power (Dig. + RF)
- Dynamic Range
- IO Data volume
- LO coherence
- Area

An ECSEL Innovation Action



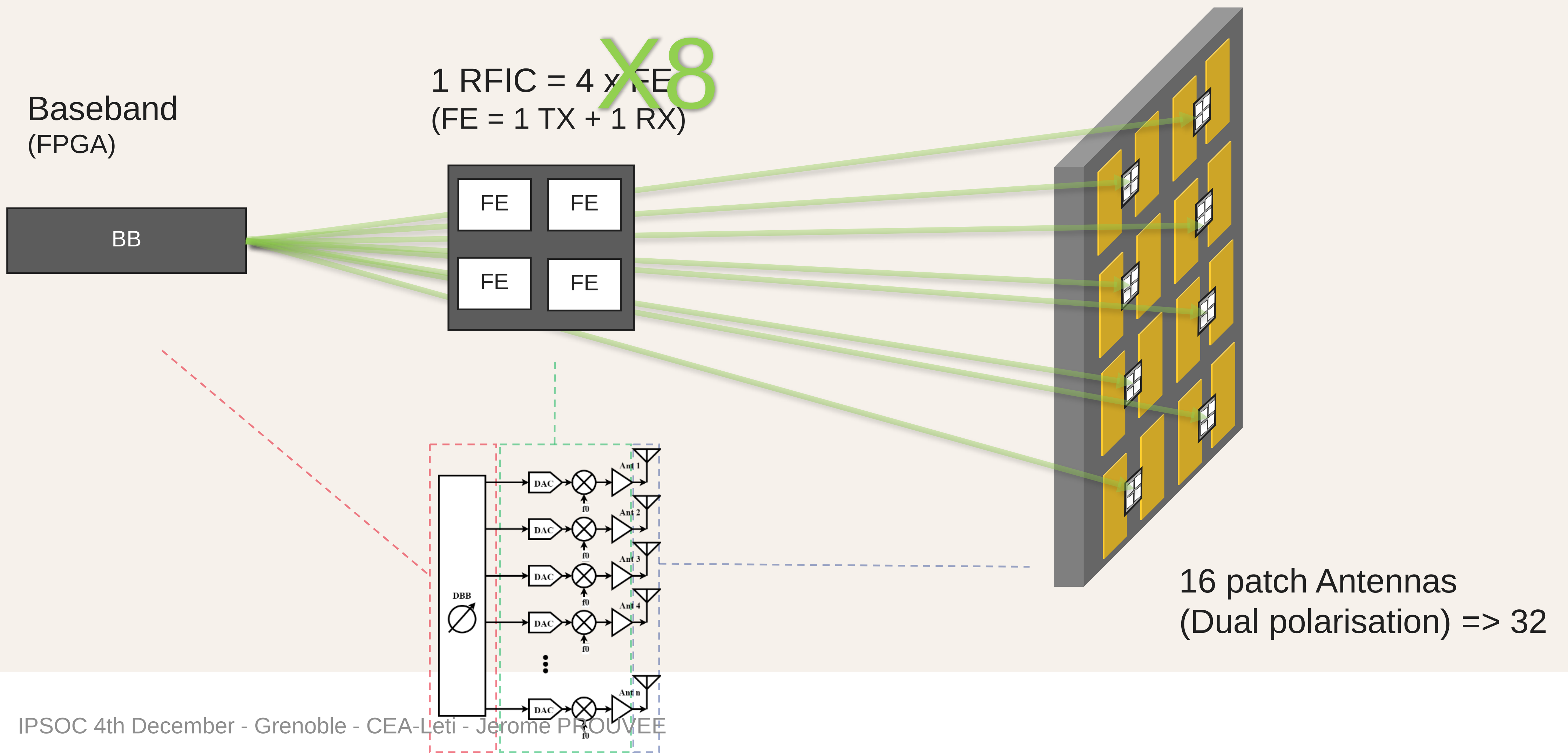


F_0= 39 GHz

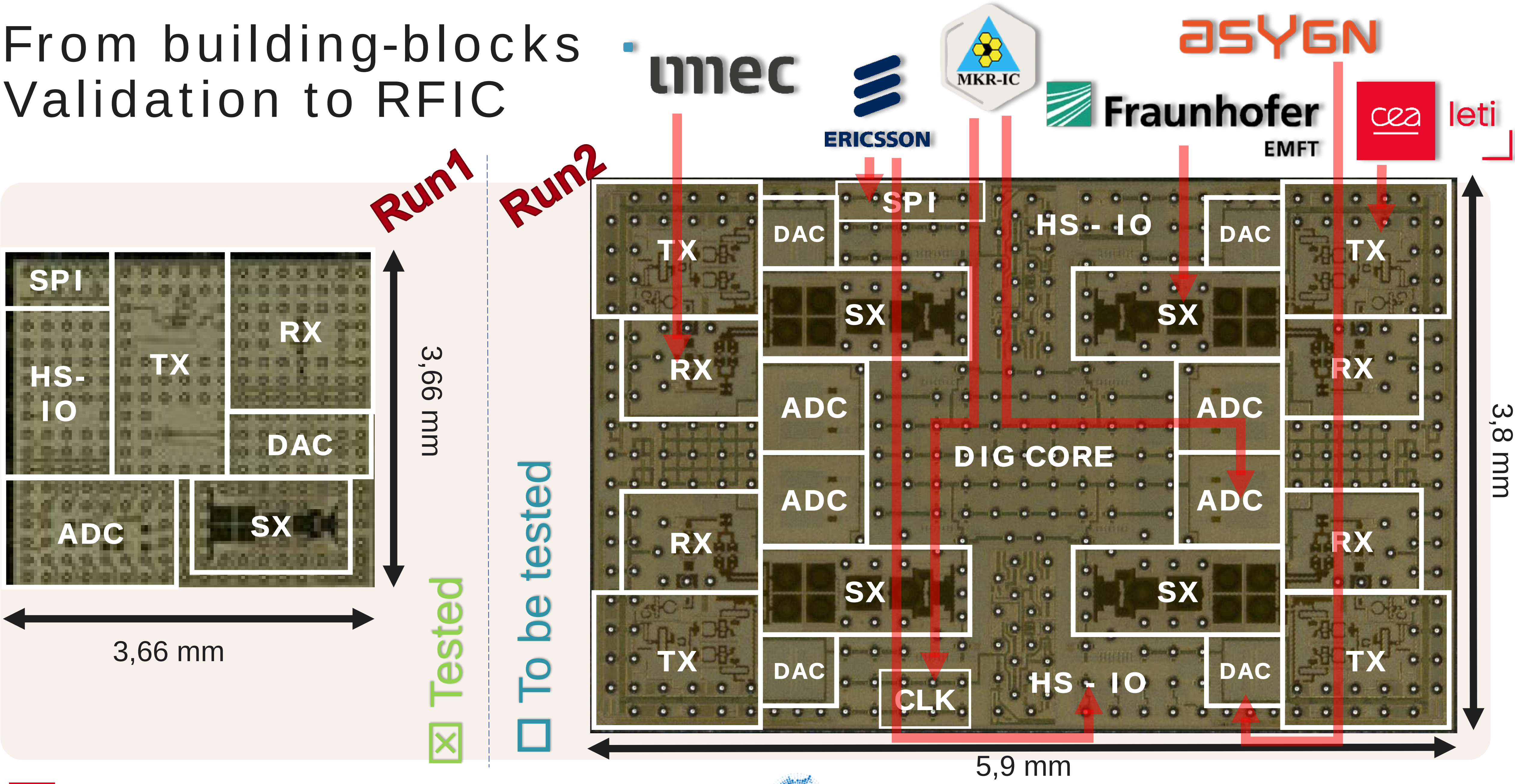
(Max BW 400 Mhz)

Illustrations Courtesy of Soitec & Ericsson

Architecture



From building-blocks Validation to RFIC

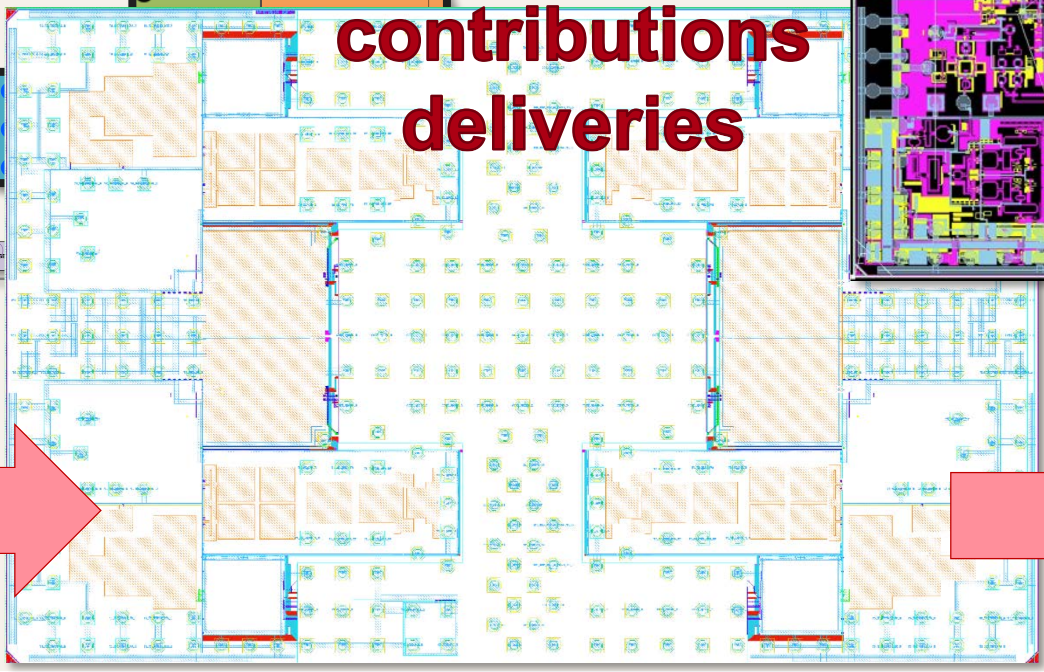


Cooperative RFIC assembly Flow

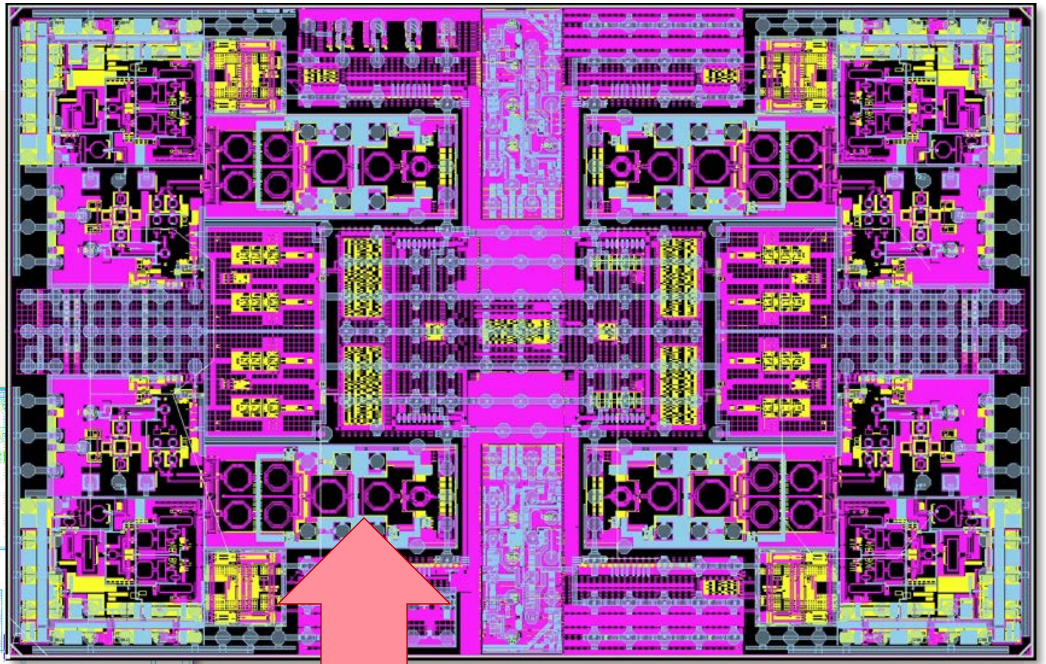
Why is automation compulsory

asygn
Top assembly

ERICSSON
Project management



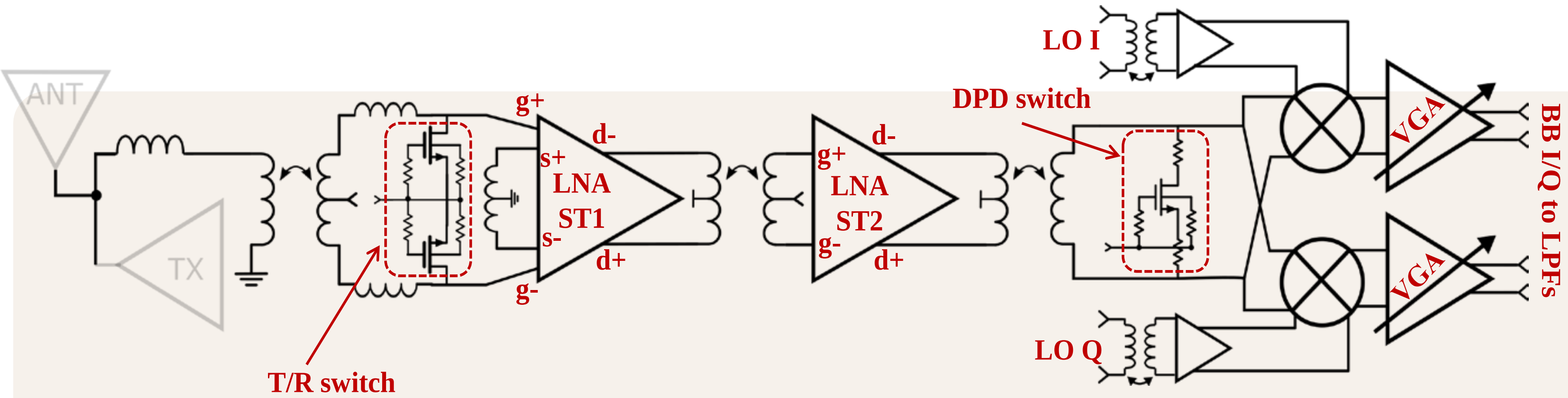
~40 contributions deliveries

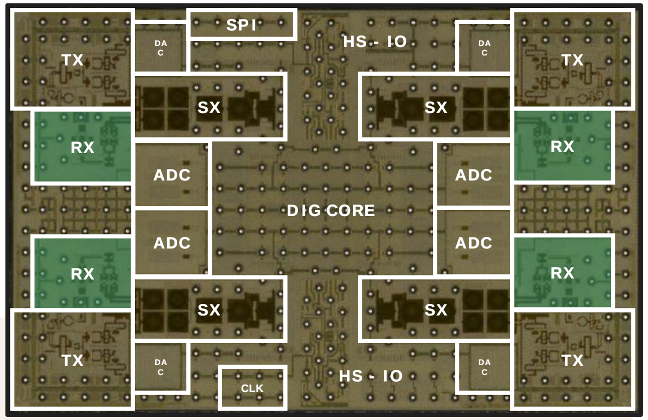


Each partners exports its netlist, GDS and abstract (subckt).

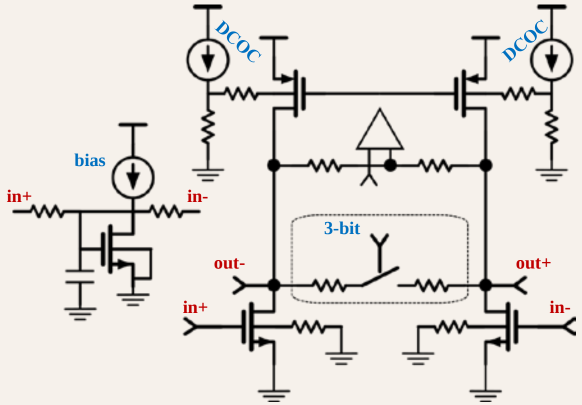
Assembling script + Hierarchical DRC/LVS

RX - LNA





- ✓ Power
- ✓ Dynamic Range
- IO Data volume
- LO coherence
- Area

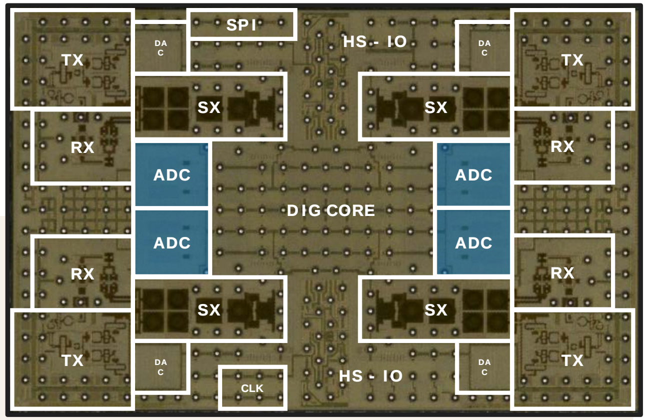


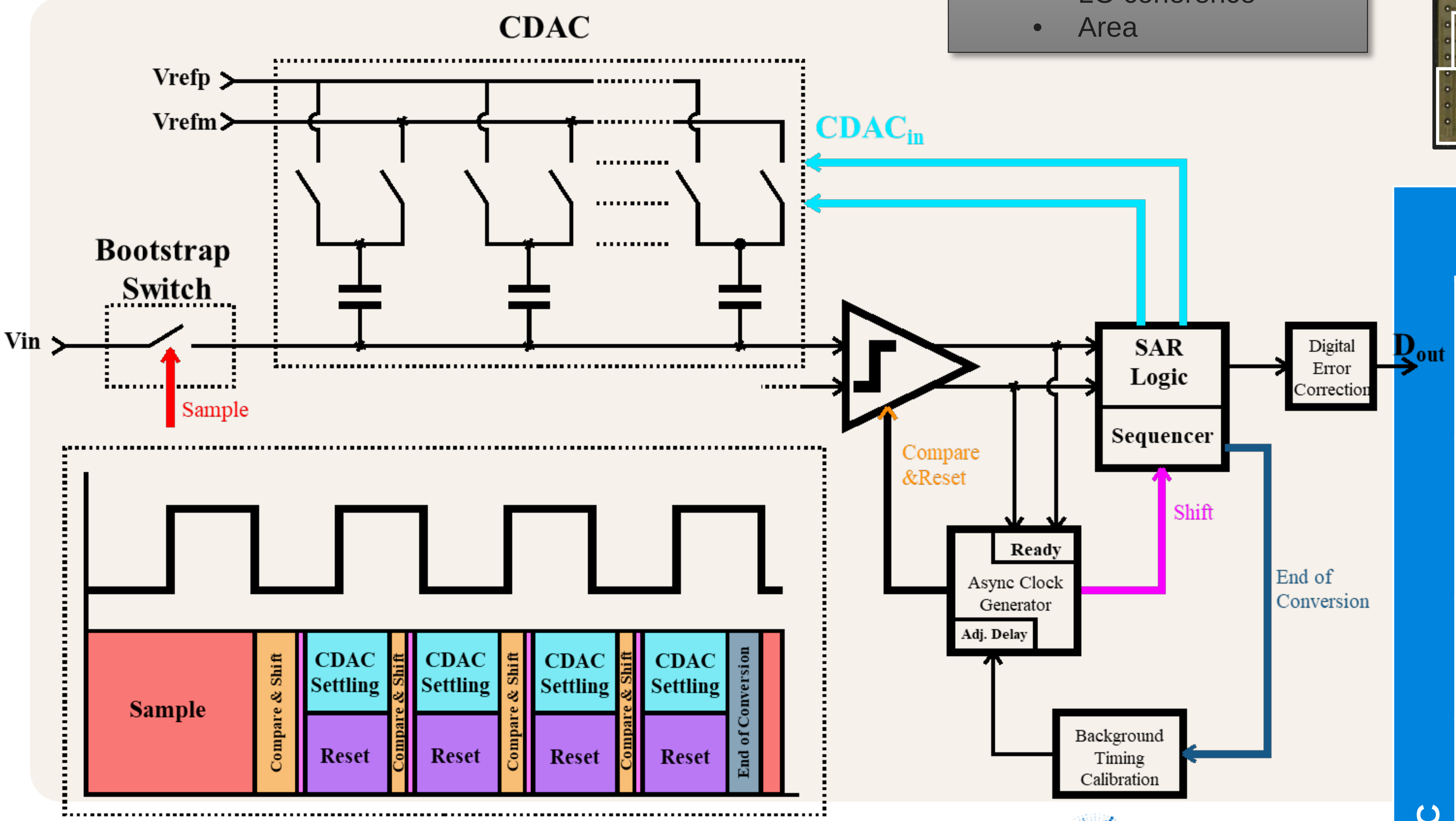
VGA gain setting	Min	Nom	Max
RX gain (dB)	17.6	23.9	28.8
VGA gain (dB)	1.7	8.1	13.0
RX NF (dB)	7.1	7.1	7.1
IIP3 (dBm)	-9.0	-9.8	-12.1

	Challenge	How did we overcome?
RX	Linearity	Pseudo differential, capacitive neutralization, source degeneration
	Power	
	Shared TX Antenna	PA “OFF” command

RX - ADC

- ✓ Power
- ✓ Dynamic Range
- ✓ IO Data volume
- LO coherence
- Area

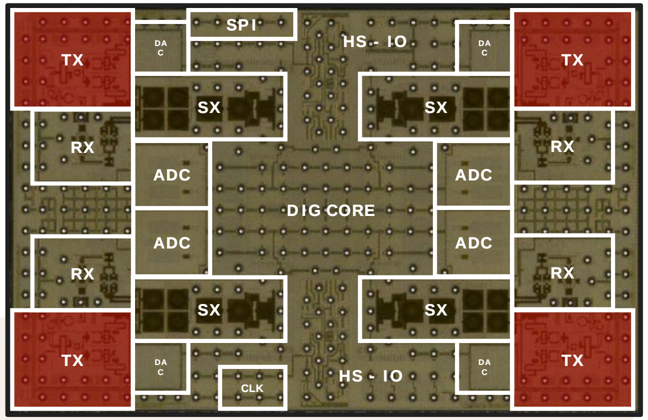




ADC	Challenge	How did we overcome?
	Energy loss (capacitive switching)	set-and-down conversion
	charge injection	bootstrapped sampling switches
	ref. voltage settling time	split-capacitor redundancy
	High frequency clock	Asynchronous control circuit

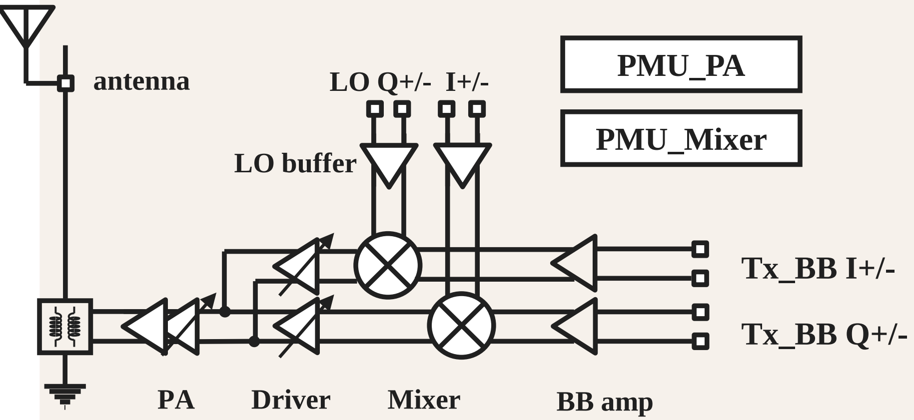
TX - RF

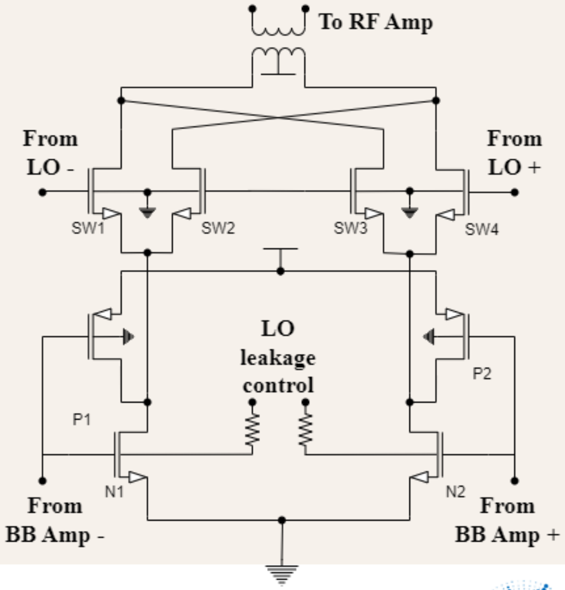
- ✓ Power
- ✓ Dynamic Range
- IO Data volume
- LO coherence
- Area

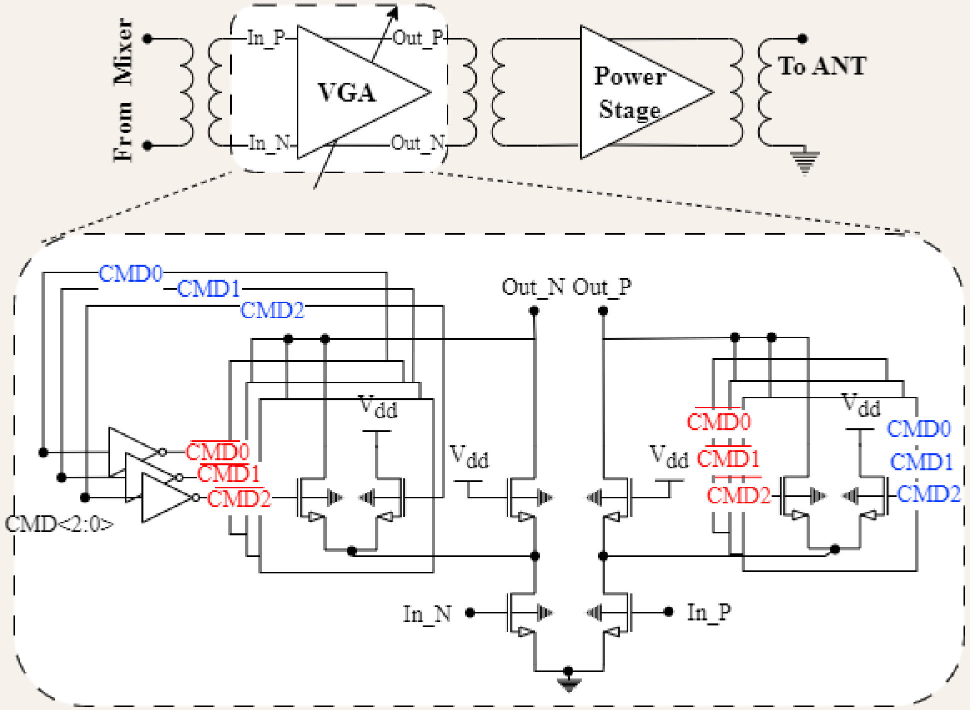


TX

Challenge	How did we overcome?
IQ mismatch	dedicated gain control for I&Q path
	full digital reconfiguration features and node power sensing
LO Leakage	FDSOI backgate use
Tx/Rx supply noise	dedicated PMUs

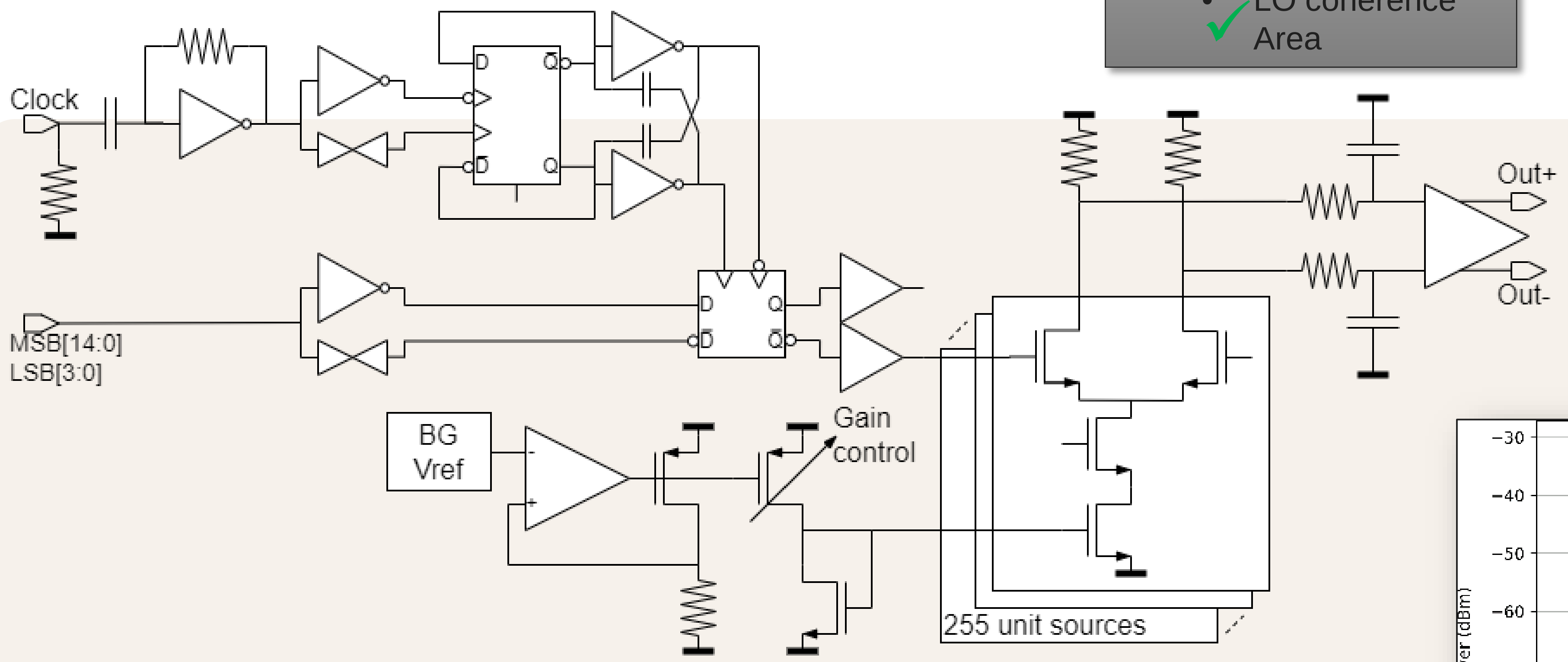


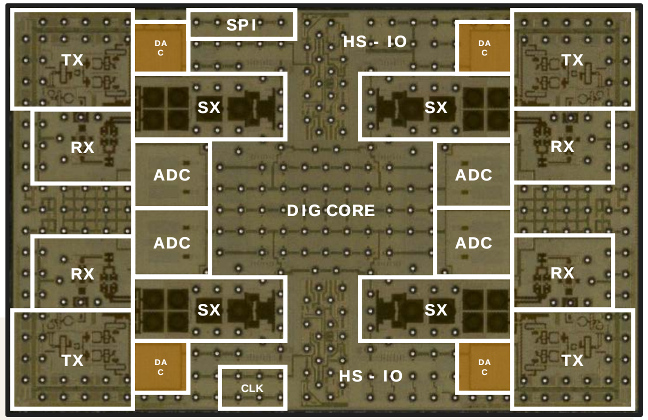


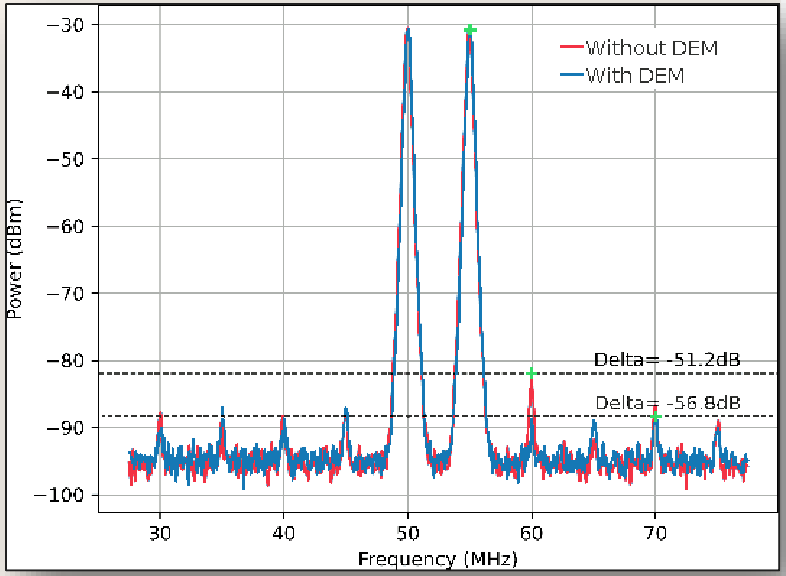


TX-DAC

- ✓ Power
- ✓ Dynamic Range
- ✓ IO Data volume
- ✓ LO coherence
- ✓ Area







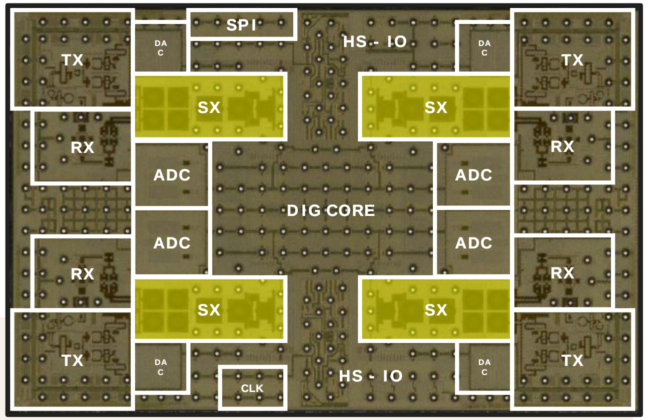
DAC

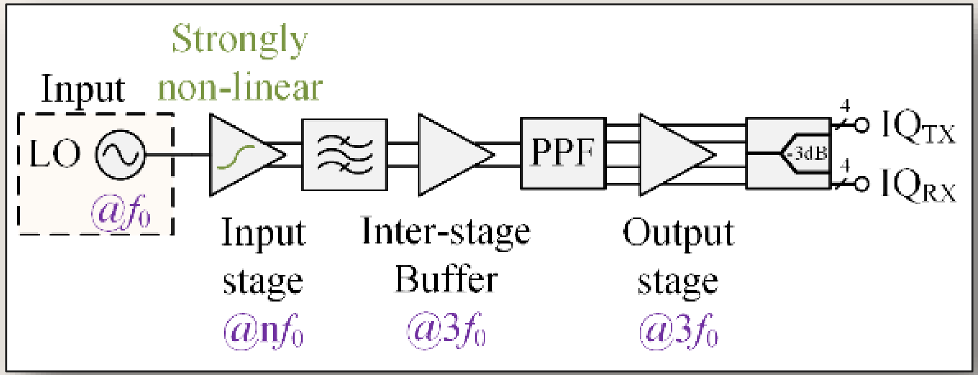
Challenge	How did we overcome?
Linearity	Dynamic Element Matching (DEM) system.
Speed	Matching +compactness driven Layout

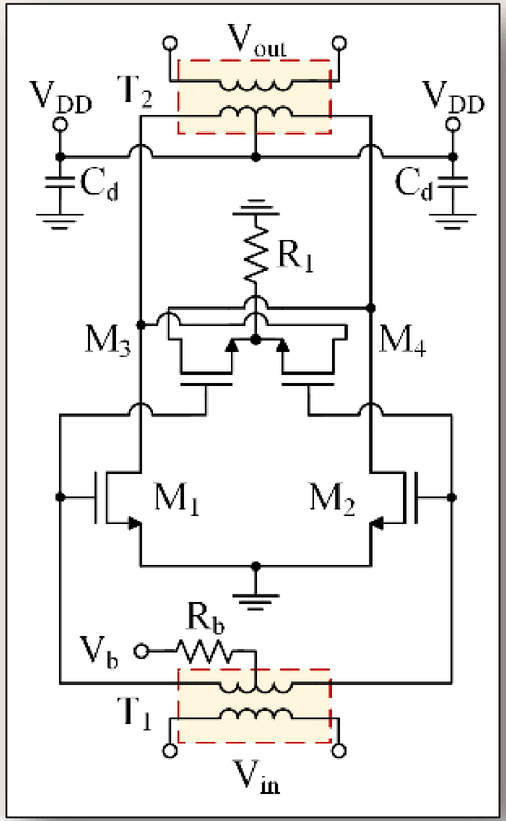
SX

Fraunhofer EMFT

- ✓ Power
- Dynamic Range
- IO Data volume
- ✓ LO coherence
- Area



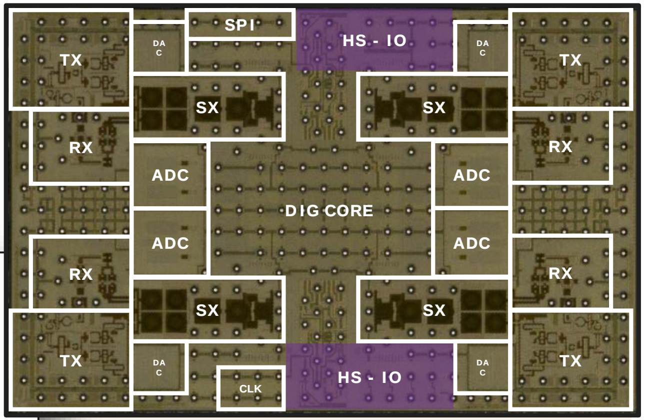


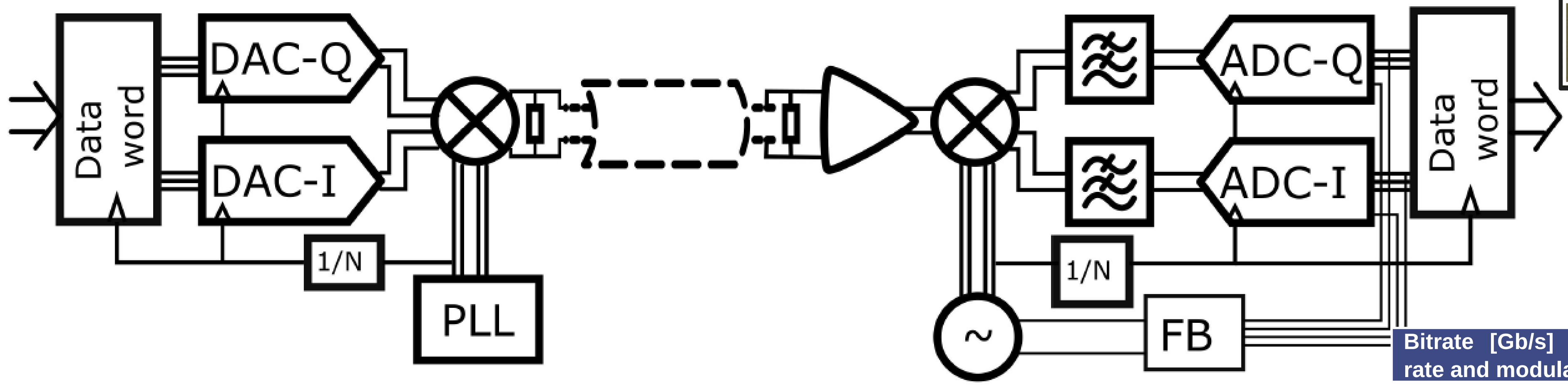


SX	Challenge	How did we overcome?
	LO to RF coupling	13 GHz multiplication
	LO coherent distribution	
	"Non-3rd" harmonics rejection	Inter-stage Buffer
	IQ generation	Polyphase filter

HS- IO

- ✓ Power
- Dynamic Range
- ✓ IO Data volume
- LO coherence
- Area





Block power dissipation [mW]	Typ
Tx (DACs,Mixer)	6.8
TxPLL	13
Rx (Amp,Mixer,Filters,ADCs)	11
RxPLL	16.5
In total	47.3

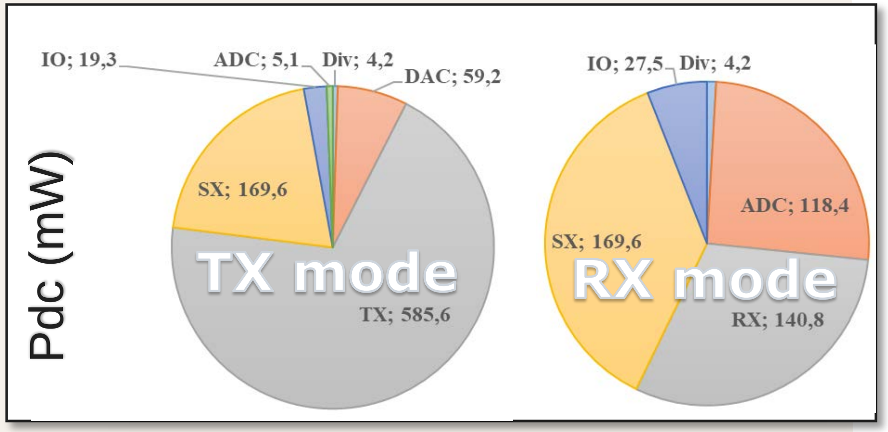
Bitrate [Gb/s] vs symbol rate and modulation	QAM4	QAM16	QAM64
3.93 GS/s	7.9	15.7	23.6
2.95 GS/s	5.9	11.8	17.7
2.36 GS/s	4.7	9.4	14.2
1.96 GS/s	3.9	7.9	11.8
1.47 GS/s	2.95	5.9	8.9
0.74 GS/s	1.75	2.9	4.4

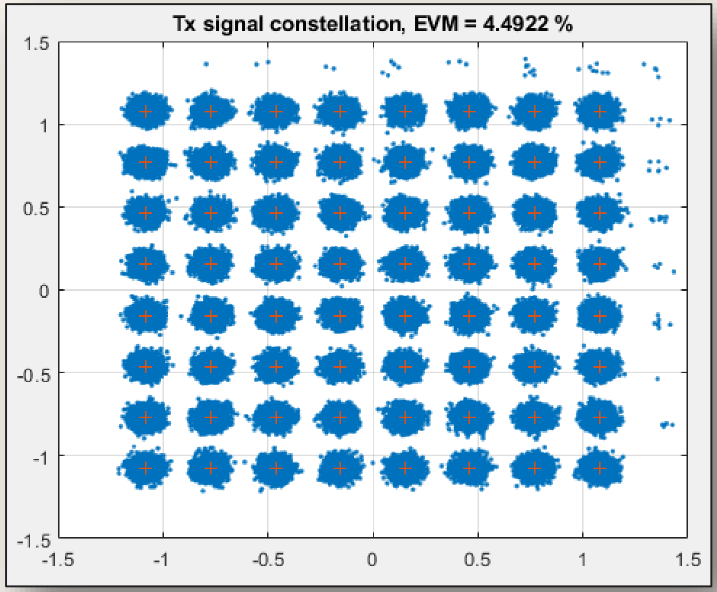
HS-IO	Challenge	How did we overcome?
	Amount of data	Alternative narrow band modulation
	Energy efficiency	
	PCB footprint	

Energy per bit [pJ/bit] vs symbol rate and modulation	QAM4	QAM16	QAM64
3.93 GS/s	5.9	3.0	2.1
2.95 GS/s	7.9	4.0	2.7
2.36 GS/s	9.9	5.0	3.4
1.96 GS/s	11.8	6.0	4.1
1.47 GS/s	15.8	8.0	5.4
0.74 GS/s	31.5	15.4	10.6

Performances (forecast)

Parameter		Min	Typ	Max	Unit
Radio Channel	n260	37	38,5	40	GHz
Number of Front-Ends (antennas) per IC			4		/
Operating temperature range	$T_{JUNCTION}$	0		100	°C
Size			22,4		mm²
Total Chip Power consumption	RX mode		461		mW
	TX mode		843		mW
Channel Bandwidth (Max = Analog BW)			50	75	MHz
Output Power	Pout		0		dBm
Effective Isotropic Radiated Power	EIRP			24	dBm
Receiver dynamic range		-86		-28	dBm
Base band sampling frequency	RX		240	250	MHz
	TX		600	700	MHz
IO data rate	downlink		150		Mbps
	uplink		225		Mbps
Adjacent Channel Leakage Ratio (ACLR)	Absolut Limit			-20	dBm/Hz
Total TX EVM (64 QAM – 10m)			4,50	5,94	%

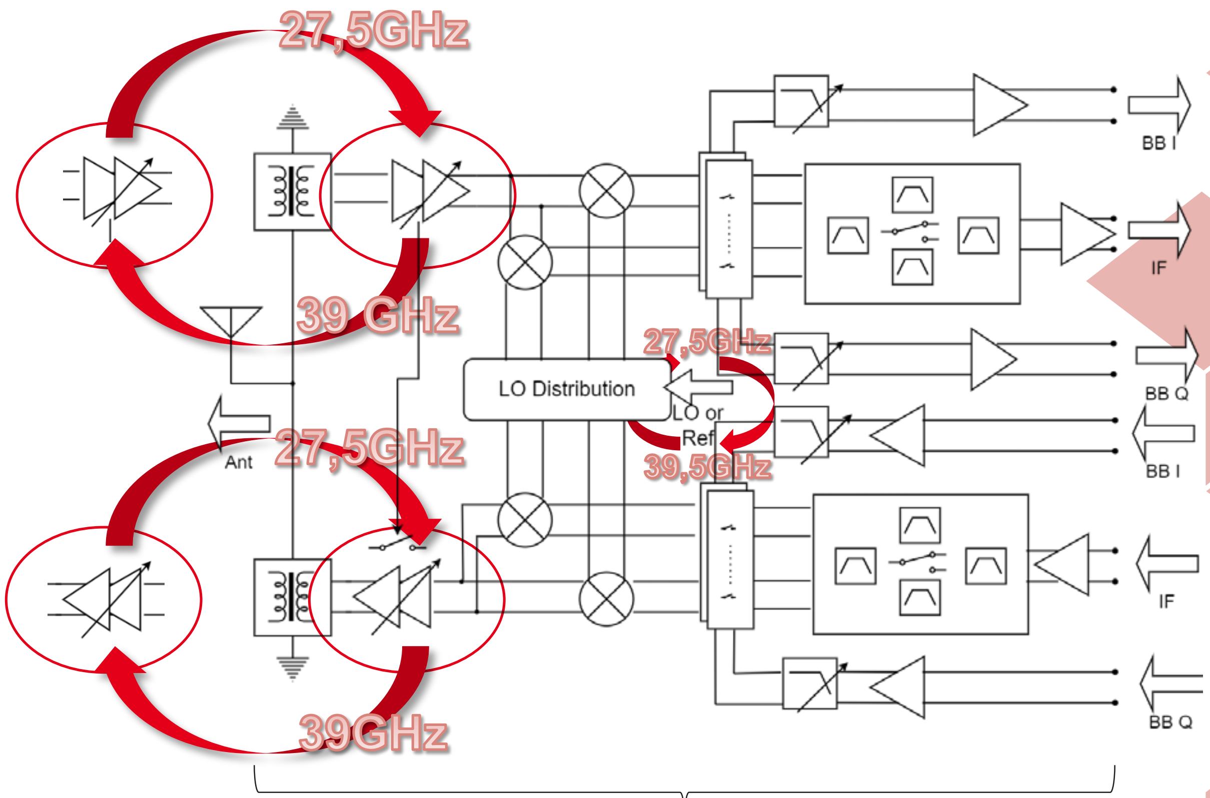




MmWave Beamforming IC State of the Art

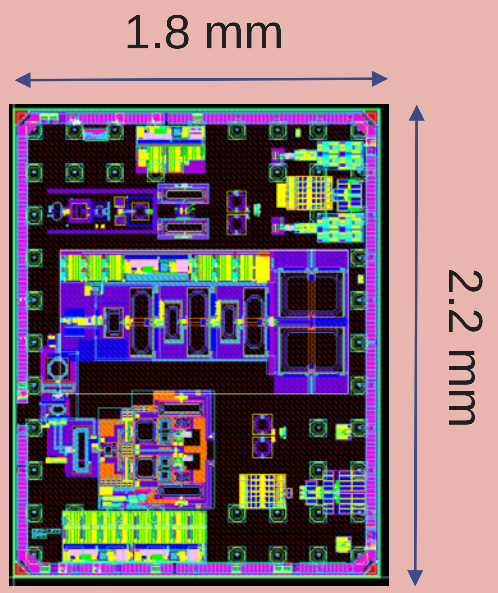
Ref	Beamforming	Freq - GHz	Area – mm²	Architecture	channel Per IC	Technology	RX Pdc -mW	TX Pdc - mW
[Dal Maistro]	analog	24.2-30.5	17	TRX	4	130nm SiGe BiCMOS	1600	1800
[Roy]	analog	37-40	17.2	TRX	8	28nm RF-CMOS	78.5/ ch	339/ch
[Dosluoglu]	digital	52.5	3.3	RX+ADC+Dig Beamformer	4	28nm RF-CMOS	96/ch + 372	/
[Mondal]	hybrid	25-30	3.86	RX	8	65nm CMOS	340	/
[Cho]	analog	26.5-29.5	30.08	TX	16	28nm CMOS	/	1630
[Johnson]	digital	28	5.76	RX+Mux	4	65nm CMOS	60/ch	/
[Kodak]	analog	62	441	TRX+ADC/DAC	64	180nm SiGe BiCMOS	4500	5125
[Alhamed]	analog	17.1-52.4	12.5	TX	4	180nm SiGe BiCMOS	/	240/ch
[Lu]	digital	28	7.73	RX+IO	16	40nm CMOS	2800	/
[Park]	analog	39	30+33.4	TRX+IF transc.	16	28nm + 65nm CMOS	624	1680/1840
This Work	digital	39	22.42	TRX+ADC/DAC+IO	4	22nm FDSOI CMOS	461	843

And Beyond Beyond5 ?

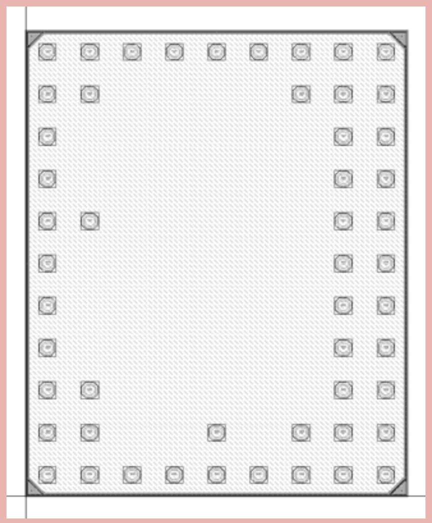


MAGMA: Millimeter wAve diGital beaMforming plAtform

end 2024:
@39GHz



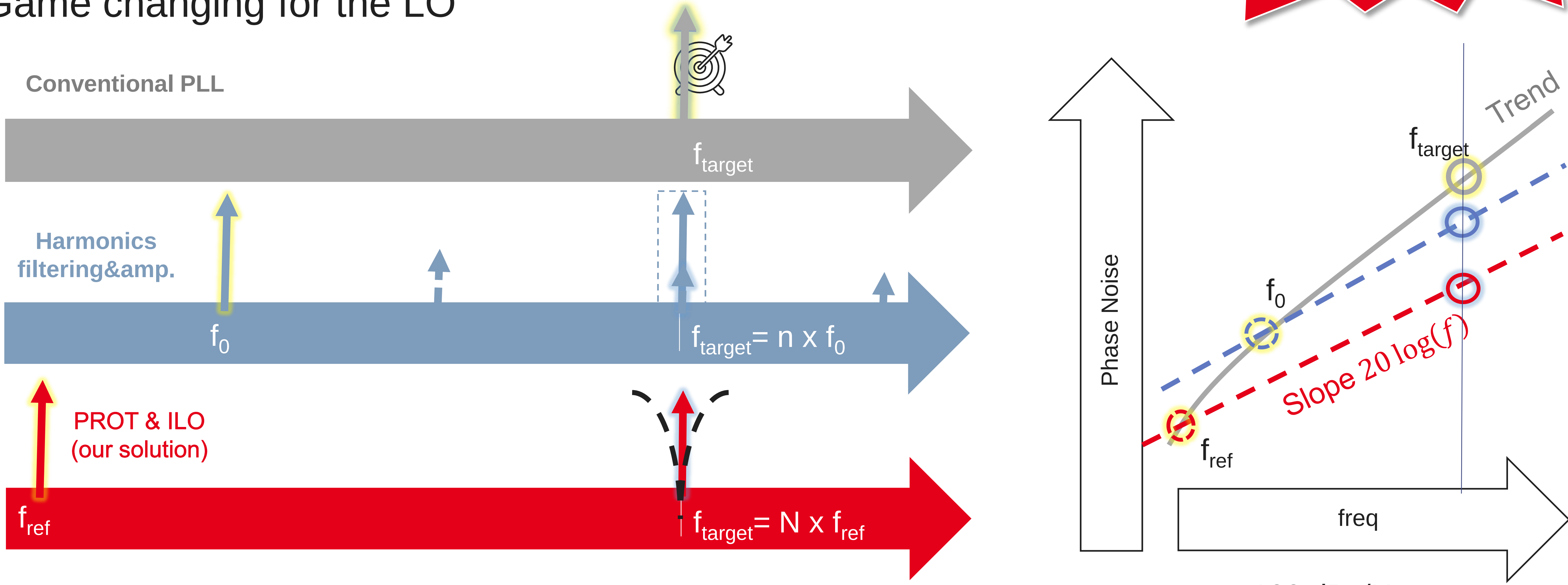
end 2025:
@27,5+39GHz
(PEPR5G)



PROT mmWave Signal generation

LO coherence

Game changing for the LO



- ✓ f_{REF}=1,25 GHz < f_0=13 GHz
- ✓ N= 29/30 > n=3

Easy to stay coherent

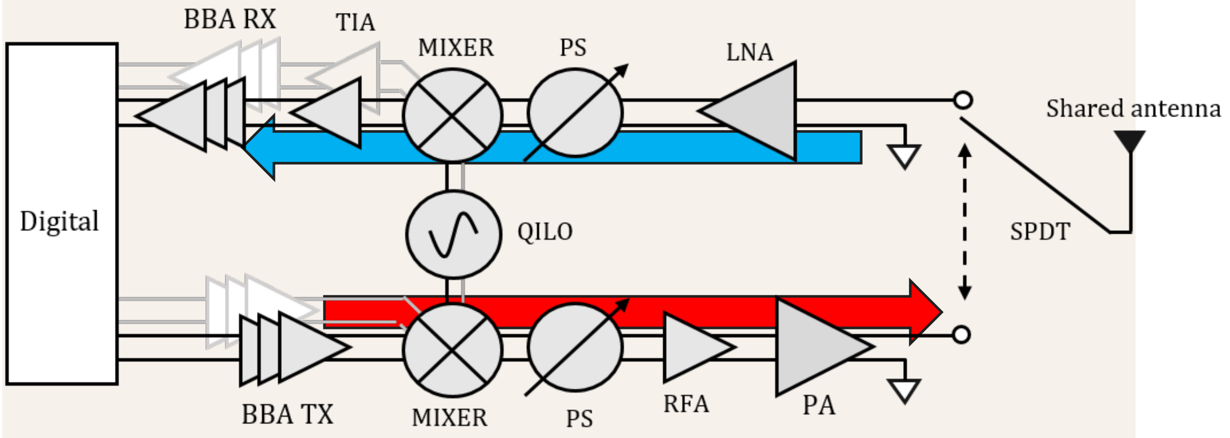
+ State of the Art Phase Noise

<100 dBc/Hz
@1MHz offset
@60GHz center freq

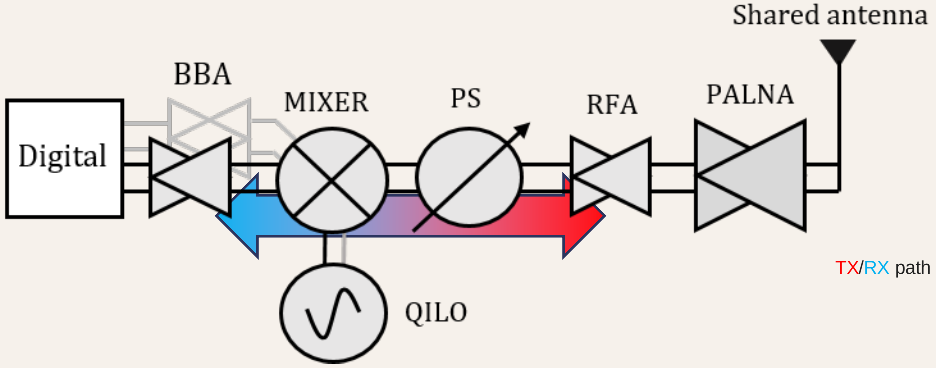
Bidirectional trx for beamforming–*Ongoing PHD*

Area

Conventional solution



Bidirectional solution



Area | **Switching losses**

Area | **Need for trade off (power efficiency)**

About 30% area saving

- Power
- Dynamic Range
- IO Data volume
- LO coherence
- Area

Digital Beamforming is a realistic strategy thanks to:

Innovative RF IC design techniques

Key enabling technologies : FD-SOI

Research for industrial innovation

Special Thanks to…

- « Design and Reuse » & E.Isa for this IPSOC opportunity
- RFIC contributors: G. Mangraviti, B. Debaillie, P. Wambacq, D. Borggreve, R. Ciocoveanu, H. Fredriksson,P. Paliwal, F. Tillman, H. Terlemez, B. Dündar, V. Pinon, F. Hasbani, A. Ferret, C. Dehos, A. Hamani, B. Martineau, D. Morche
- W. Buchholtz and Globalfoundries for MPW manufacturing
- D. Eckbert for project leadership

ECSEL Joint Undertaking

KDT JU KEY DIGITAL TECHNOLOGIES JOINT UNDERTAKING

The Key Digital Technologies Joint Undertaking - the Public-Private Partnership for research, development and innovation – funds projects for assuring world-class expertise in these key enabling technologies, essential for Europe's competitive leadership in the era of the digital economy. KDT JU is the successor to the ECSEL JU program. www.kdt-ju.europa.eu

BEYOND5

The BEYOND5 "Building the fully European supply chain on RFSOI, enabling new RF domains for sensing, communication, 5G and beyond" project has received funding from the ECSEL Joint Undertaking (JU) under grant agreement No 876124. www.beyond5project.org

FRANCE 2030

anr agence nationale de la recherche AU SERVICE DE LA SCIENCE

Part of this work was funded by the French National Research Agency (ANR-22-PEFT-0005) as part of France 2030 and the NF-YACARI project.

Key References

- A. N. Uwaechia and N. M. Mahyuddin, "A Comprehensive Survey on Millimeter Wave Communications for Fifth-Generation Wireless Networks: Feasibility and Challenges," in IEEE Access, vol. 8, pp. 62367-62414, 2020, doi: 10.1109/ACCESS.2020.2984204.
- D. Dosluoglu, K. -D. Chu, D. Pena-Colaiocco, I. Zhao, V. Sathe and J. C. Rudell, "A Reconfigurable Digital Beamforming V-Band Phased-Array Receiver," ESSCIRC 2022- IEEE 48th European Solid State Circuits Conference (ESSCIRC), Milan, Italy, 2022, pp. 493-496, doi: 10.1109/ESSCIRC55480.2022.9911486.
- M. Johnson et al., "A 4-element 28 GHz Millimeter-wave MIMO Array with Single-wire Interface using Code-Domain Multiplexing in 65 nm CMOS," 2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Boston, MA, USA, 2019, pp. 243-246, doi: 10.1109/RFIC.2019.8701732.
- U. Kodak, B. Rupakula, S. Zihir and G. M. Rebeiz, "A 62 GHz Tx/Rx 2x128-Element Dual-Polarized Dual-Beam Wafer-Scale Phased-Array Transceiver with Minimal Reticle-to-Reticle Stitching," 2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Boston, MA, USA, 2019, pp. 335-338, doi: 10.1109/RFIC.2019.8701863.
- H. . -C. Park et al., "4.1 A 39GHz-Band CMOS 16-Channel Phased-Array Transceiver IC with a Companion Dual-Stream IF Transceiver IC for 5G NR Base-Station Applications," 2020 IEEE International Solid- State Circuits Conference - (ISSCC), San Francisco, CA, USA, 2020, pp. 76-78, doi: 10.1109/ISSCC19947.2020.9063006.
- G. Mangraviti, B. Debaillie and P. Wambacq, "A 39-GHz 18.5-mW LNA with T/R switch, 15.4-dB gain, -2.2dBm IIP3, 5.6-dB NF, for a 5G in-cabin basestation in 22-nm FD-SOI," 2022 24th International Microwave and Radar Conference (MIKON), Gdansk, Poland, 2022
- L. H. de Carvalho Ferreira and T. C. Pimenta, "A CMOS voltage reference for ultra low-voltage applications," IEEE ICECS, 2005.
- Y. Yi, D. Zhao and X. You, "A Ka-band CMOS Digital-Controlled Phase-Invariant Variable Gain Amplifier with 4-bit Tuning Range and 0.5-dB Resolution," IEEE RFIC, 2018.
- Y. Du et al., "A 16-Gb/s 14.7-mW Tri-Band Cognitive Serial Link Transmitter With Forwarded Clock to Enable PAM-16/256-QAM and Channel Response Detection," in IEEE Journal of Solid-State Circuits, vol. 52, no. 4, pp. 1111-1122, April 2017, doi: 10.1109/JSSC.2016.2628049.
- W. -H. Cho et al., "10.2 A 38mW 40Gb/s 4-lane tri-band PAM-4 / 16-QAM transceiver in 28nm CMOS for high-speed Memory interface," 2016 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2016, pp. 184-185, doi: 10.1109/ISSCC.2016.7417968
- Z. Jiang, H. Beshara, J. Lam, N. Ben-Hamida and C. Plett, "High Speed DMT for 224 Gb/s and Faster Wireline Transmission," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 70, no. 4, pp. 1758-1771, April 2023, doi: 10.1109/TCSI.2023.3234920.